REMARKS/ARGUMENTS

Claims 1-3 and 9 remain pending in the application. Claims 1, 2 and 9 have been amended. Applicant respectfully requests entry of these amendments since Applicant believes the amendments place the application in condition for allowance.

I. REJECTIONS UNDER 35 U.S.C. § 102

In the above referenced Office Action, the Examiner rejected Claim 9 under 35 U.S.C. § 102(b) as being anticipated by Chen (U.S. Patent No. 6,057,202). In light of the above amendments, Applicant respectfully traverses this rejection.

Applicant has amended independent Claim 9 to recite: "An on-chip inductor consisting of: a first dielectric layer; a conductive winding on the first dielectric layer; a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer; a field oxide layer having a major surface parallel to the major surface of the first dielectric layer; and a substrate having a major surface parallel to the major surface of the first dielectric layer."

Chen teaches an inductor including a single dielectric layer 12, as shown in Figure 1, three dielectric layers 22, 30 and 31 plus air layers 28/29, as shown in Figures 4 and 6, or four dielectric layers 22, 26, 30 and 31 plus air layers 28/29, as shown in Figures 3 and 5. Chen does not teach an inductor including only two dielectric layers, as presently claimed. Since Claim 9 includes the transitional phrase "consisting of," Claim 9 excludes elements other than those specifically recited. Therefore, the figures (and corresponding description) in Chen teaching three or four dielectric layers, plus air layers, do not teach Applicant's invention. And, since the embodiment shown in Figure 1 has only a single dielectric layer, this embodiment also does not teach Applicant's invention.

For the foregoing reasons, Applicant respectfully submits that independent Claim 9 is in condition for allowance. Accordingly, Applicant respectfully requests that the Examiner withdraw the §102 rejection of Claim 9.

II. REJECTIONS UNDER 35 U.S.C. § 103

In the above referenced Office Action, the Examiner rejected Claims 1-3 and 9 as being unpatentable over Grzegorek (U.S. Patent No. 5,760,456) in view of Zhu (U.S. Patent No. 6,133,079). In light of the above amendments, Applicant respectfully traverses these rejections.

Applicant has amended independent Claim 1 to recite: "An on-chip inductor consisting of: a first dielectric layer; a conductive winding on the first dielectric layer; a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer; a P-well having a major surface parallel to the major surface of the first dielectric layer; and a substrate having a major surface parallel to the major surface of the first dielectric layer."

In addition, Applicant has amended independent Claim 2 to recite: "An on-chip inductor consisting of: a first dielectric layer; a conductive winding on the first dielectric layer; a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer; a P-well having a major surface parallel to a major surface of the first dielectric layer; a field oxide having a major surface that is juxtaposed to the major surface of the P-well; and a substrate having a major surface parallel to the major surface of the first dielectric layer."

Furthermore, Applicant has amended independent Claim 9 to recite: "An on-chip inductor consisting of: a first dielectric layer; a conductive winding on the first dielectric layer; a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer; a field oxide layer having a major surface parallel to the major surface of the first dielectric layer; and a substrate having a major surface parallel to the major surface of the first dielectric layer."

Grzegorek teaches an inductor including only a single dielectric layer (insulating layer 18). Grzegorek does not teach or suggest that the inductor could include two dielectric layers.

Moreover, as Applicant previously argued, since Claims 1, 2 and 9 each include the transitional phrase "consisting of," these claims exclude elements other than those specifically recited.

Zhu teaches a reduced capacitance inductor as shown in Figures 4-7 and described in column 4, line 33, through column 5, line 33. As shown in Figure 4 and described in the corresponding text, the inductor region 22 includes an inductor coil 60 (which is formed on second and third metallization layers 57 and 59), a first IMD (inter-metal dielectric) 55, a second IMD 58, an ILD (inter-layer dielectric) 52, a FOX (field oxide) layer 50, a p-well 28, an n-region 24, and a substrate 20.

Thus, the inductor of Zhu, to achieve lower capacitance, includes multiple dielectric layers (IMD 1, IMD 2, and ILD), a field oxide layer (FOX), a p-well 28, and an n-region 24. Since Zhu's inductor, which includes more elements (as listed above) than that of any of Claims 1, 2, 4 and 9, Zhu also does not teach or suggest the inductor of Claims 1, 2 and 9. As such, the combination of Grzegorek and Zhu does not teach or suggest the inductor of Claims 1, 2 and 9.

For the foregoing reasons, Applicant respectfully submits that independent Claims 1, 2 and 9 (and all claims dependent therefrom) are in condition for allowance. Accordingly, Applicant respectfully requests that the Examiner withdraw the §103 rejections of Claims 1-3 and 9.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126 (Ref. BP2108).

Respectfully submitted,

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